Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VCC**
2. **AOUT**
3. **AIN**
4. **BOUT**
5. **BIN**
6. **COUT**
7. **CIN**
8. **VSS**
9. **DIN**
10. **DOUT**
11. **EIN**
12. **EOUT**
13. **SELECT**
14. **FIN**
15. **FOUT**
16. **VDD**

**.100”**

**13 12 11 10**

**14**

**15**

**16**

**1**

**2 3 4 5 6 7**

**9**

**8**

**11901A**

**MASK**

**REF**

**.069”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 1190A**

**APPROVED BY: DK DIE SIZE .069” X .100” DATE: 8/17/21**

**MFG: HARRIS THICKNESS .000” P/N: CD4504B**

**DG 10.1.2**

#### Rev B, 7/1